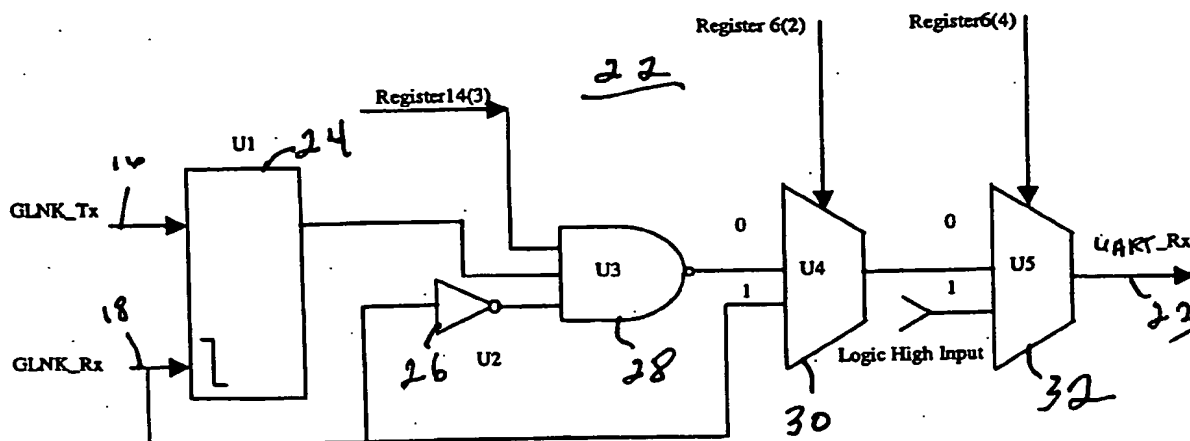


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Digital Control Circuit							
Mode	CPLD Control Registers			CPLD Data Inputs		UART Input	Comments
Setup #	Register6(4)	Register6(2)	Register14(3)	GLNK_Tx	GLNK_Rx	UART_Rx	
1 (Mode 1)	0	0	1	1	X	=GLNK_Rx	Default Setting
2 (Mode 1)	0	0	1	0	X	LOGIC 1	Default Setting
3 (Mode 1)	0	0	0	X	X	LOGIC 1	IR Blaster Active
4 (Mode 2)	0	1	0	X	X	=GLNK_Rx	Configuration Test Mode
5 (Mode 3)	1	X	X	X	X	LOGIC 1	DETECTED DEMO PIN

X: don't care if level is logic high or low

FIG. 3B

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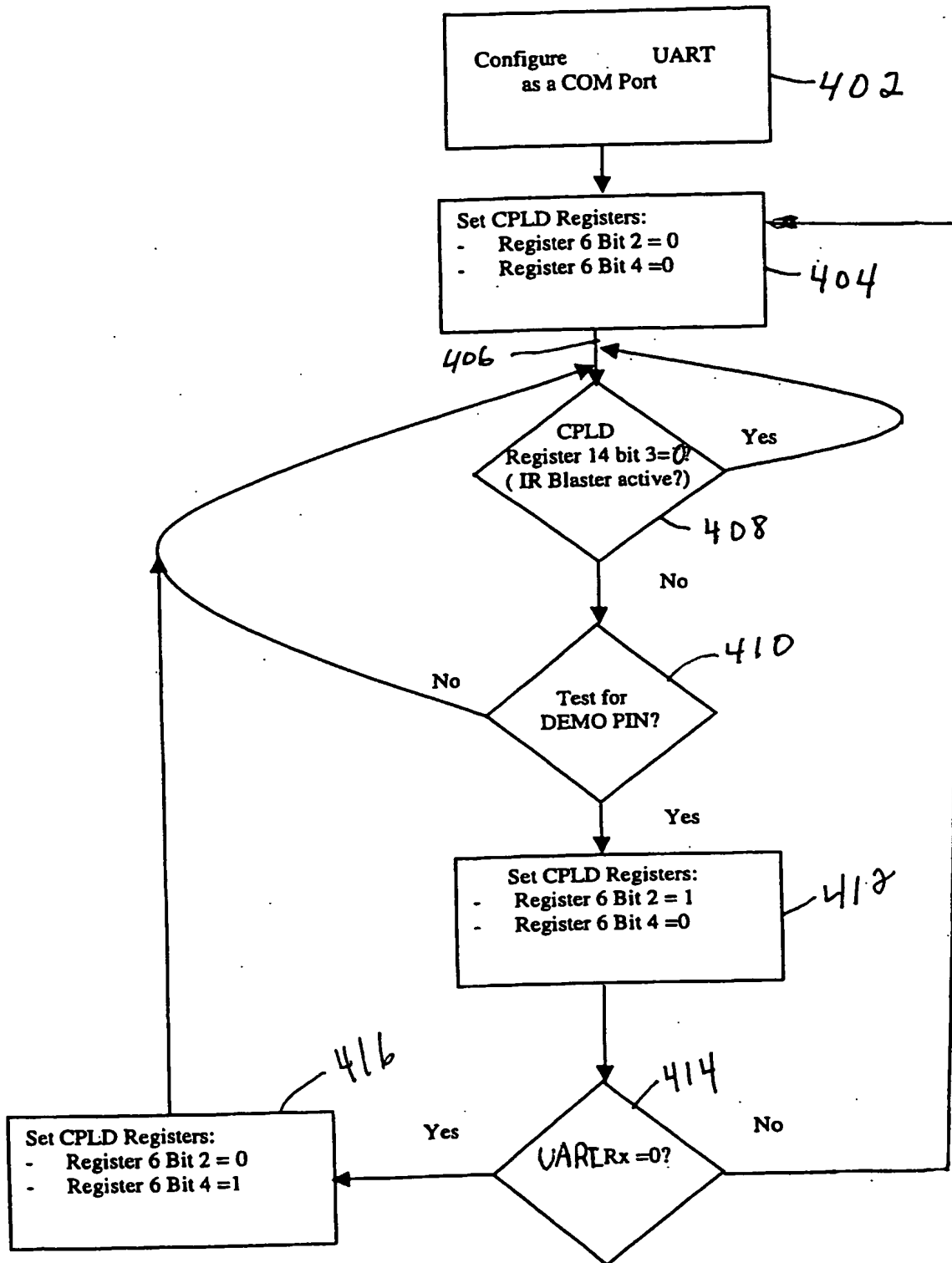


FIG. 4

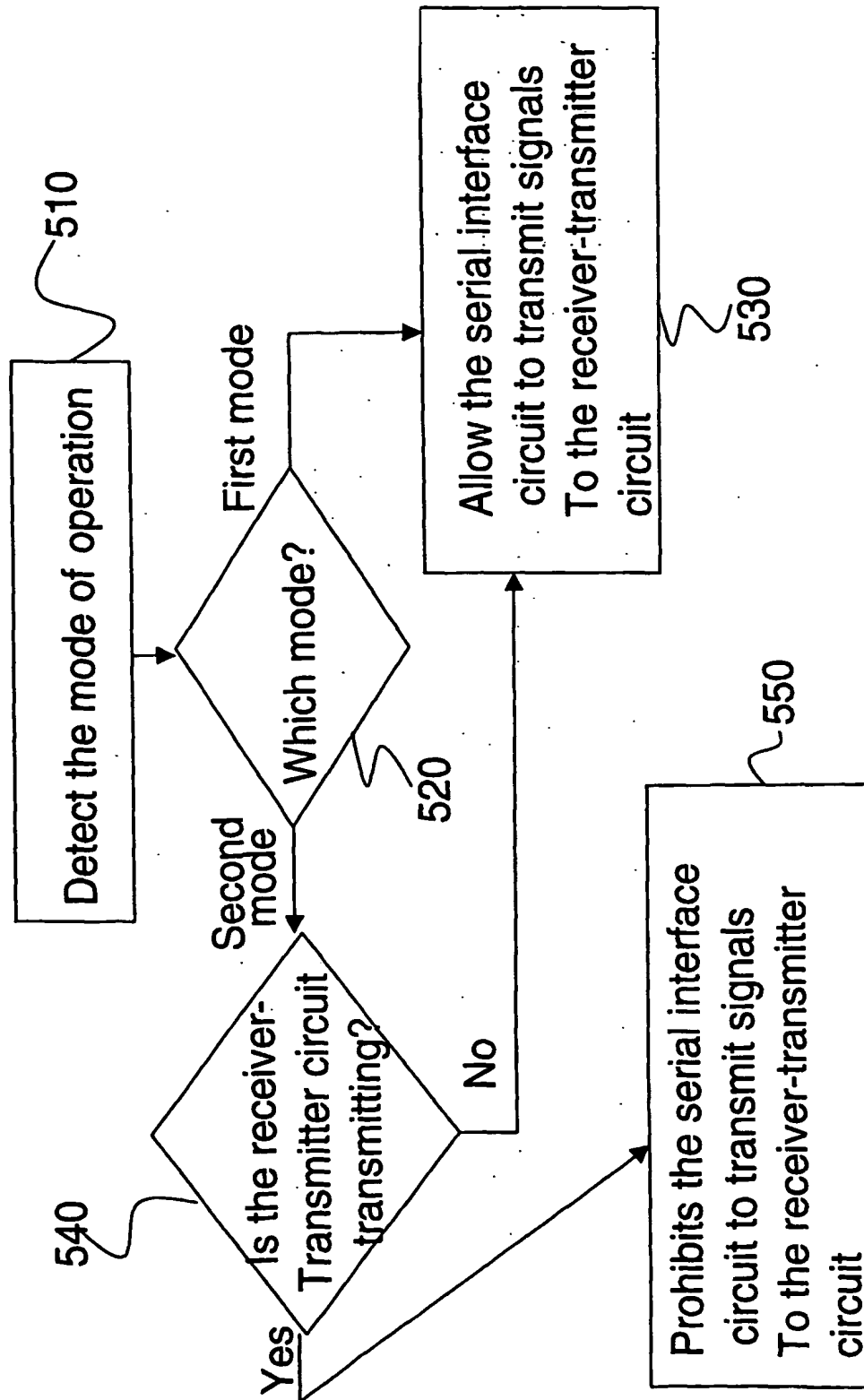


FIG. 5

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